Evolution of Wireless Communication along with Encoders

Rashmi R, Manju Devi

Abstract: ***Now a days technology drastically increasing, leads to increase in communication also. Internet of Things (IOT) is very basic fundamental necessary to the consumers in this decade, which requires a communication path mainly from end to end. By understanding this technology growth, took as motivation and started a survey for turbo decoder architecture in Long Term Evolution (LTE) and 3GPP-LTE communication. Different generation technologies adopt different kinds of encoder as well as decoder to encrypt the data which can be sent from source devices to destination devices, which consists parameters like data rate, frequency used to transmit and speed of transitioning i.e., encoding and decoding the data at the transmitter as well as receiver. This paper represents a survey on different architectures of turbo decoder in LTE communication which can give a brief idea about the communication and also the usage of turbo encoder in various applications. Initially we look back a history and development of a communication system till LTE. Later we discuss the different technologies and topologies on turbo decoder along with its architecture, advantage and disadvantage.***

Keywords : IOT, LTE, Turbo Encoder, Communication, Encoding and Decoding

I. INTRODUCTION

Wireless communication is the communication between the two or more systems or points that are not connected through electrically. The radio waves are used in the most common wireless technologies. Cellular network communication is a kind of addicted technology and also widely accepted technology in a current generation, which is also be a very good research area for researchers. The LTE communication system is not the initial development of communication system and also turbo decoder is not the initial decoder. Lot of researchers are under research to increase the communication speed between the two different systems and also to optimize it. The main agenda of this paper is to understand the previous research work and to extract the problems or disadvantage intact to it.

II. HISTORY OF TELECOMMUNICATION

In Africa, America and some in some parts of Asia the telecommunication was begun by using the smoke signals and drums. Semaphore telegraphy is the early communication system using pivoting shutter and tower system to convey the information by Visual signals and information is encoded by the positioning of mechanical elements. The French scientist named Claude chappe invented Semaphore telegraphy in 1792. This system was constructed using a wooden bean to show the symbols and communication was established between Lille and Paris.

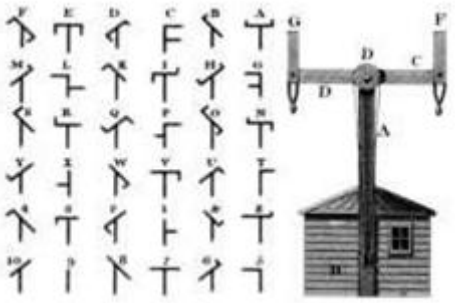

Fig1: Chappe telegraphy and code of letters and symbols associated with it.

Fig 1 represents the Chappe telegraphy model and code of letters and symbols associated with it. Later in 1726 electrical communication system initially unsuccessful where the great scientists like Laplace, Gauss and Ampere were involved in invention. In 1816 the scientist and inventor Sir Francis Ronalds invented first working telegraphy with the help of static electricity. Later in 1838 William Fothergill cooke and Charles wheat stone patented a six wire and five needle system and it is commercially available to customers to communicate around 21 kilometre (KM). This is the first electromagnetic telegraphy mounted on a device. Also in 1838, Samuel Morse and Alfred Vali combined electrical telegraphy and logging device (recording message on paper tape). This Morse telegraphy was simple and highly efficient by Morse coding and the same coding is précised by Hoffman code over 100 years later in digital communication. This technology was spread over 32000 KM in United States (US).

Fig 2 and Fig 3 represents the Morse code receiver along with recording on paper tape as well as the comparison of current standard with Morse code. Later in 1878-79 Alexander Graham Bell invented electrical telephone based on harmonic telegraphy. This technology was expanded between the two countries that is United States (US) and United Kingdom (UK). G. G. Hubbard and Alexander G. Bell were started the first company on telephone named Bell telephone company in US, now it is American Telephone and telegraph (AT&T), largest voice device communication company in world till now.

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The first voice communication call which is transcontinental occurred on 25th January 1915,

Fig 2: Morse code receiver along with recording on paper tape

Fig 3: Comparison of current standard with Morse code

it was commercially marketed across globe, transatlantic voice communication was impossible to customers until 1927. In 1880 Alexander G Bell and C. S. Tainter experimentally achieved the world‟s first wireless telephone voice call by photophones with modulated lightbeams projected, which was implemented in military and optical fibre communication. Finally in 1956, the operational first transatlantic telephone cable which would has more than 100‟s of electronic amplifiers came into exist (before the six years of Telstar launch). The static Public Switched Telephone Network (PSTN) relay for telephone calls by land line telephones to earth station which was communicated via geostationary satellite. In 20th century the technology was improvised and the communication was done through submarine communication cables by using optic fibre cables. Later in 1979 the satellite communication technology is drastically impacted with a host of commercial satellites for mobile phones, Radio‟s, Television‟s and internet access. Later in 1990‟s, satellite communication price keeps on dropping significantly. In early 2004, Japan proposed the LTE for the first time internationally with data speed of 144Mbits/s. In 2007, Infineon found the first RF transceiver which supports LTE functionality on a chip with RF silicon processor in CMOS logic. In 2011, the researchers under gone lot of research and found a 4G LTE in south Asia (Srilanka) with a data speed of 96MBits/s. The above section can insist the brief survey of wired and wireless telephone communication and also incorporates the drastic development in the technology along with significant decrease in the price of communication. Further we explain the specific functionality of decoders which are main part of communications and also their application along with demerits of it. The agenda of this survey is to get the at most solution for the various demerits of Turbo encoder in the present LTE technology. In 2019 there were in and around 717 operators who have launched LTE networks across globe as per Global Mobile Suppliers Association (GMPS) survey.

III. IMPLIMENTATION OF TURBO CODER AND DECODER ARCHITECTURE FOR VARIOUS REAL TIME APPLICATIONS

The various applications like finding the maximum or minimum number a large number set, MAP decoder, mobile WiMAX and 3GPP-LTE, LTE communication and so many. In this paper we try to interpret some real time applications and usage of Turbo coder as well as decoder.

A. Field Programming Gate Array (FPGA) implementation by using parallel high speed Maximum A Posterior (MAP) decoders, in this work, the aim is to implement the designed FPGA for High speed parallel architecture for MAP probabilities decoder. Turbo principle is used by turbo equaliser to perform the digital communication. The turbo decoding can achieve a close performance of Shannon‟s theoretical limit and also improves the performance of the digital communication receiver. The very high throughput can be achieved by building a sliding window approach by parallel systolic scheme. Maximum of 1.6 Gb/s is achieved by implementing a 8-state MAP decoder which need to place at the receiver end. MAP decoder is the optimised technique to minimise the bit error rate (BER). Due to this reason and results, it can be used in the mitigate channel impairments which can be found in the high speed optical fibre. To conclude the overall architecture is to achieve a throughput of 1.6Gbps with the help of 8 state max-log-Map equalizer for commercial GPP 4 channel, also provides the increase in the speed of communication as its future scope. Table 1 refers the comparison of different soft in/soft out (SISO) decoders throughput. Fig 4 represents the systolic architecture that is been implemented with 8-state max-log-MAP [1].

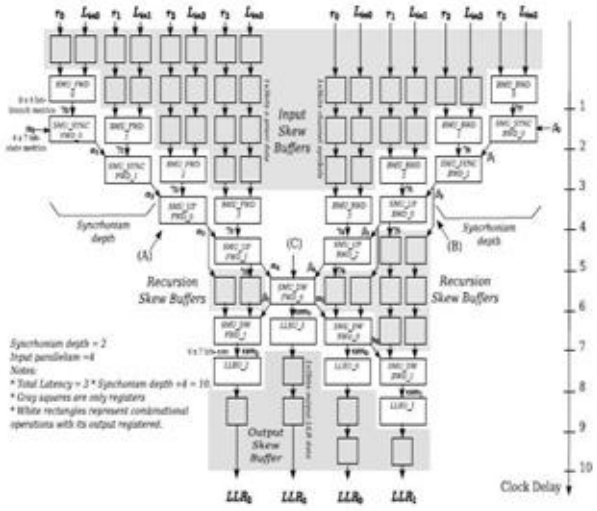

Fig 4: Implemented Systolic 8-state max-log-MAP architecture

B. Parallel Radix-4 Uniform turbo decoder for 3GPP-LTE technology as well as mobile WiMAX technology are been implemented to give support the current 4G wireless communication. In this approach the new hard-core sharing hardware architecture which consists of 8 retimed radix-4 SISO decoder. This architecture enables good throughput and two modes of parallel hardware interweavers to support the regular permutation (ARP) and quadratic polynomial permutation (QPP) interleaver. Fig 5 represents the Overall architecture of Radix-4 Uniform turbo decoder with multiplexing in time. In parallel turbo decoding system is the single chip and it has a collusion free access for the ARP or QRP interleaver which is been defined in WiMAX/3GPP-LTE standards for mobiles. Here each SISO decoder in parallel turbo decoder accesses particular memory by finding a specific address computed in the interleavers. In conventional add-compare-select (ACS) block the cascade the two-input ACS has a drawback of more time consumption as well as limiting operating frequency. For this, applying a retiming as well as migrating of common operator can reduce the time consumption by enabling the turbo decoder to perform operations in high frequency and also provides higher throughput. The memory sharing was achieved with by radix 4 Uniform single binary turbo decoding which interchanges the two extrinsic data values. Finally the two hardwares are combined by using dual mode hardware interleaver, which consists of WiMAX as well as 3GPP-LTE on a single chip. By using two accumulator based circuit, the exact value of flip flop will disables the mobile WiMAX mode. The results of those decoders exhibits 100Mb/s in case of 8 iterations and also throughput can also made more in case of future work [2].

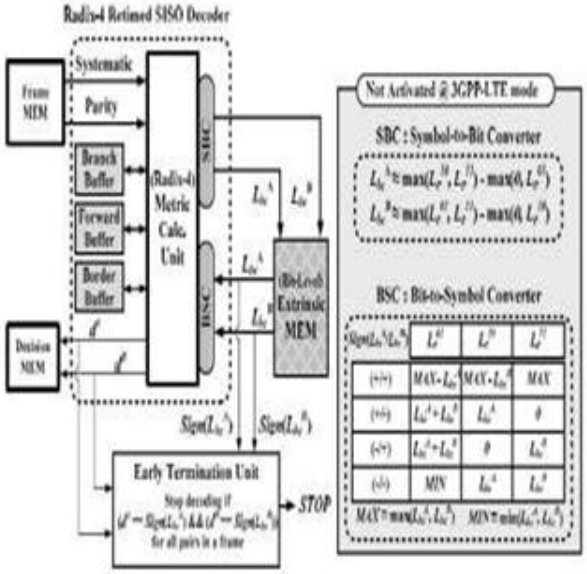

Fig 5: Overall architecture of Uniform turbo decoder with time multiplexing

Table 1: Throughput comparison between different SISO detectors

Sl No.	Tech	Clock	Throughput 1 iteration	Algorithm
1	180n	145MHz	144Mbps	log-MAP
2	Virtex	310MHz	139Mbps	MAX scale
3	Virtex	56MHz	79.2Mbps	MAP
4	180n	500MHz	500Mbps	SOVA
5	130n	750MHz	750Mbps	log-MAP
6	Virtex	100MHz	1.6Gbps	max-log MAP

C. As turbo code reduces the received error signals in LTE channel and optimization of this turbo code takes good field of research. In the year 2011, the new innovative and optimize 8-level turbo encoder algorithm is designed along with VLSI architecture for LTE. Also this architecture is based upon 3GPP standards and employs dual RAM turbo code interleaver, optimize 8-level parallel architecture, efficient 8-level index generator and recursive pair matching. The recursive pairwise matching technique used here to minimize the quantity of additions. The dual RAM in turbo code interleaver reduces the clock latency.

D. An 3rd order reconfigurable energy efficient continuous time ∑Δ modulator is presented which can be applicable for 4G-LTE system. By switching between feed forward (FF) and feed backward (FB) in the flexibility architecture, the power consumption is reduced hence it is introduced in all the core blocks (amplifier, feedback DAC and multi-bit quantizer). The FF has a drawback of high speed indispensible summing block in spite of that it has a less output swing with power efficient integrator in it. FB architecture has a capacity of enabling roboust NTF design which required for 3rd order reconfigurable ∑Δ modulator in FF architecture.

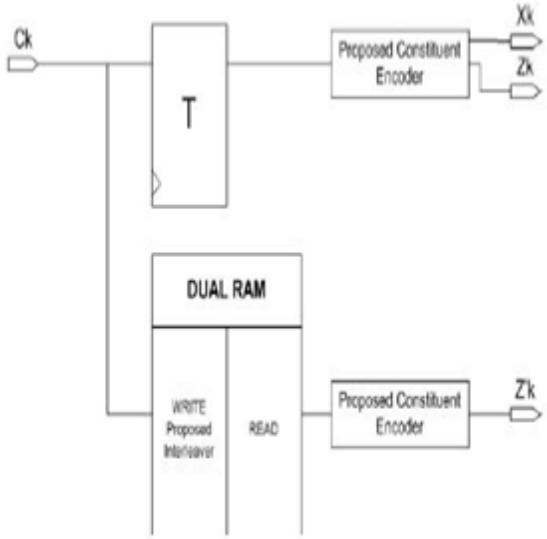

Fig 6: Block diagram of Turbo encode architecture

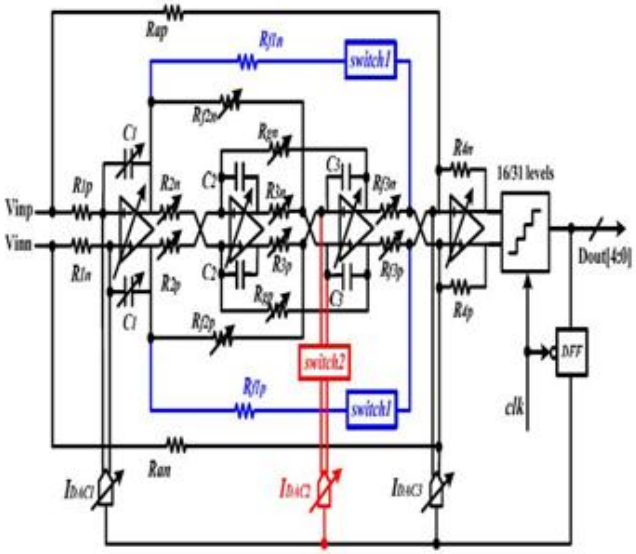

Fig7: 3rd- order reconfigurable ΣΔ modulator architecture

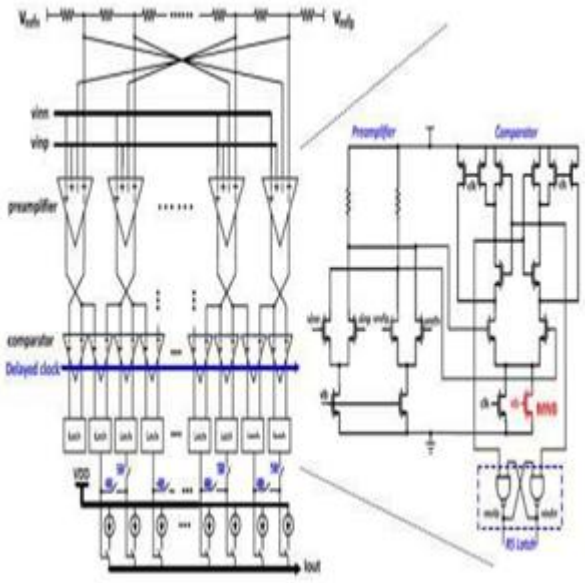

Fig 8: Flexible architecture of multi bit quantiser and FB DAC

Fig 7 represents the architecture of 3rd-order reconfigurable ΣΔ continuous time modulator. Fig 8 represents the Flexible architecture with multi bit interpolating quantiser along with FB DAC. Finally, the architecture is implemented by using 130nm CMOS Technology, the modulator results are 5/10/15/20 MHz over SNR of 72.7/ 66.7 /60 /59 dB for 1.2V and the Power consumed is 8/14.7/16/21 mW. The future scope is to extend the reconfigurable signal bandwidth range [4].

E. High speed architecture to find a generic min/max values, which address is presented. The proposed method is extended from earlier work on LZC architecture. Also this method explains about quantum cellular architecture (QCA), which provides considerable advantage in terms of frequency of clock and power consumption. In this proposed architecture, to obtain the gth best value in the random list of „k" elements, and g value will be any value between 1 to k. This search of the value is important part in iterative channel decoder. It is an efficient hardware with less complexity as well as less latency, when the co-ordinates of the unsigned set of „k" larger values. The results are obtained after synthesis with a 90nm CMOS standard Cell Technology which provides the best specific values for g and k. The QCA is also used for regulation and scalable properties, which reduces lower power and high speed. To achieve all these certain topologies were taken in to consideration, on a first stage each of the k element has 2^n bits with one hot code , this hot code determines the maximum value and in 2nd stage add of maximum value is determined. These two stages describes the leading zero counter (LCZ). A pipeline version of this architecture also achieved by increasing the throughput and also longer latency at the same cost with clock period of 0.32nsec. Fig 9 represents the internal architecture of decoder [5].

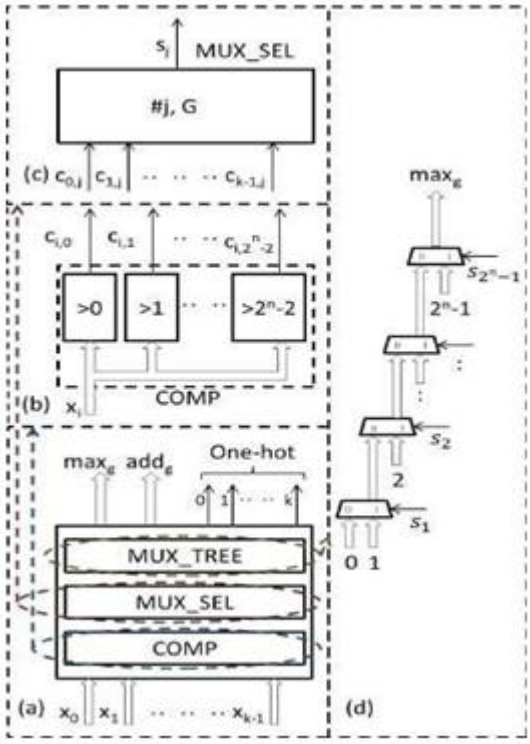

Fig 9: (a) Overall Architecture and main units, b) Parallel Comparators, (c) Signal select on Generation and (d) Multiplexer

IV. CONCLUSION

The overall aim of this paper is to brief out the evolution of the wireless communication system along with encoder. Here initially we have approached to explain the stage by stage growth in wired communication system to wireless communication system along with associated data coders and decoders. In further section, discussion of some important real time implemented architectures and algorithms for Turbo coder and decoder which needed for current generation (4G), 3GPP, WiMAX technologies. The main drawback of turbo coder is high decoding latency.

The main challenges present in turbo coding architecture are:

i. More time consumption due to iterative nature of the decoding algorithm.
ii. MAP decoders recursion in forward or backward flow.
iii. The interleavers/deinterleavers units between MAP decoder.

Finally tracking these problem statements and to provide the optimised solution to them will be future scope, it enables the less time and more latency to LTE communication system with better data rates.

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